

WHAT IS CLAIMED IS:

1. An apparatus comprising:

an integrated circuit (IC) mounted on a chip carrier, the IC having one or more differential pair circuits coupled thereto, the chip carrier having a signal escaping portion and a remaining portion; and

differential signal lines coupled to the differential pair circuits, the differential signal lines (i) extending through the chip carrier and (ii) having first and second segments;

wherein the first segment extends through the escaping portion and the second segment extends through the remaining portion; and

wherein the first and second segments have respective first and second widths.
2. The apparatus of claim 1, wherein the escaping portion is configured for escaping transmitted signals from the IC.
3. The apparatus of claim 1, wherein the first and second widths provide substantially uniform impedance characteristics across the signal lines.
4. The apparatus of claim 3, wherein the impedance is within a range of about 90 to 110 ohms.

5. The apparatus of claim 1, wherein the second width is larger than the first width.

6. The apparatus of claim 1, wherein the differential signal lines include respective inverting and non-inverting paths; and

wherein the paths along the escaping portion are separated by a first spacing and the paths along the remaining portion are separated by at least a second spacing.

7. The apparatus of claim 6, wherein the second spacing is larger than the first spacing.

8. The apparatus of claim 6, wherein the first and second spacings cooperate to reduce cross-talk between the inverting and non-inverting paths.

9. The apparatus of claim 6, wherein the first and second widths and the first and second spacings are determined based upon modeling and simulations.

10. The apparatus of claim 1, wherein the signal lines are configured to transmit high data rate signals.

11. The apparatus of claim 10, wherein a data rate of the high data rate signals is greater than or equal to about 5 gigabits per second.

12. The apparatus of claim 6, wherein the inverting and non-inverting paths are adjacent to one another.

13. An integrated circuit (IC) (i) having a differential circuit coupled thereto and (ii) mounted on a chip carrier, the differential circuit including a signal escaping portion and a remaining portion, the IC comprising:

differential signal lines extending through the chip carrier and including first and second segments;

wherein the first segment extends through the signal escaping portion and the second segment extends through the remaining portion;

wherein the first and second segments have respective first and second widths; and

wherein the first and second widths provide substantially uniform impedance characteristics across the signal lines.

14. The IC of claim 13, wherein the first and second widths provide substantially uniform impedance characteristics across the signal lines.

15. The IC of claim 13, wherein the second width is larger than the first width.

16. The IC of claim 13, wherein the differential signal lines include respective inverting and non-inverting paths; and

wherein the paths along the escaping portion are separated by a first spacing and the paths along the remaining portion are separated by at least a second spacing.

17. The IC of claim 16, wherein the second spacing is larger than the first spacing.

18. The IC of claim 17, wherein the first and second spacings cooperate to reduce cross-talk between the inverting and non-inverting paths.

19. The IC of claim 18, wherein the first and second widths and the first and second spacings are determined based upon modeling and simulations.

20. The IC of claim 13, wherein the signal lines are configured to transmit signals having a data-rate greater than about 5 gigabits per second.